

DDR SDRAM Module Code Information(1/2)

Last Updated : April 2009

M X X X X X X X X X X X X X X X X X X

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory Module(M)

2. Module Configuration

3 : 4/8 Byte DIMM 4 : 4/8 Byte SODIMM

3~4. Data bit

- 11 : x72 184pin VLP Registered DIMM
- 12 : x72 184pin 1U Register DIMM
- 28 : x72 208pin Register DIMM
- 32 : x32 160pin U-DIMM
- 37 : x72 240pin Non-JEDEC Registered DIMM
- 38 : x72 276pin Register DIMM of Socket Type
- 46 : x72 294pin Register DIMM with PLL
- 47 : x72 294pin Register DIMM with PLL
(512MB DIR2)
- 48 : x72 276pin Register DIMM of Socket Type Tall
DIMM
- 58 : x72 276pin Register DIMM (Low profile)
- 63 : x64 172pin uDIMM
- 64 : x64 160pin U-DIMM
- 68 : x64 184pin U-DIMM
- 70 : x64 200pin U-SODIMM
- 71 : x64 204pin U-DIMM
- 81 : x72 184pin U-DIMM
- 83 : x72 184pin Register DIMM
- 85 : x72 200pin U-DIMM
- 88 : x72 200pin Register DIMM

* VLP : Very Low Profile

5. Feature, Voltage

L : DDR SDRAM, 2.5V

6~7. Depth

- 09 : 8M (for 128Mb/512Mb)
- 16 : 16M 17 : 16M (for 128Mb/512Mb)
- 32 : 32M 33 : 32M (for 128Mb/512Mb)
- 64 : 64M 65 : 64M (for 128Mb/512Mb)
- 28 : 128M 29 : 128M (for 128Mb/512Mb)
- 56 : 256M 57 : 256M (for 512Mb)
- 51 : 512M 52 : 512M(for 512Mb)

8. # of bank in Comp., Interface, Refresh

- 1 : 4bank, SSTL_2, 64m/4K Refresh (15.6us)
- 2 : 4bank, SSTL_2, 64m/8K Refresh (7.8us)

9. Composition Component

- 0 : x4 3 : x8 4 : x16
- 6 : x4 Stack (83+56 DSP)
- 7 : x8 Stack (83+56 SDP)
- 8 : x4 Stack
- 9 : x8 Stack

10. Component Generation

- M : M-die A : A-die
- B : B-die C : C-die
- D : D-die E : E-die
- F : F-die G : G-die
- H : H-die J : J-die
- L : L-die N : N-die

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M X X X X X X X X X X X - X X X X X
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

11. Package

D : FBGA (Lead-Free, Larger) F : WFP (Lead-Free)
P : POC R : WLP
S : FBGA (Smaller)
K : TSOP2 (400mil) (DDP)
T : TSOP2 (400mil)
U : TSOP2 (400mil) (Lead-Free)
L : TSOP2 (Lead-Free, Halogen-Free)
N : sTSOP
V : sTSOP2 (Lead-Free)
6 : sTSOP2 (Lead-Free, Halogen-Free)
G : FBGA
Z : FBGA (Lead-Free)
H : FBGA (Halogen-Free, Lead-Free)

12. PCB Revision & Type

0 : Mother PCB 1 : 1st Rev.
2 : 2nd Rev. 3 : 3rd Rev.
4 : 4th Rev.
B : Non Heat Spreader
E : Embedded PCB Design
L : Low Cost
M : New PC2700
N : Non ECC U-DIMM PCB
P : Custom PCB
S : Reduced Layer PCB
Q : Custom PCB (OSP+Dummy Pad)
R : Custom PCB (OSP+ParityOpt)
U : 0.72 INCH PCB DIMM

13. "—"

14. Power

C : Normal, Self Ref. L : Low, Self Ref.
K : Reduced, Self Ref.

15~16. Speed

A0 : 10ns@CL2 A2 : 7.5ns@CL2
AA : 7.5ns@CL2, TRCD2, TRP2
B0 : 7.5ns@CL2.5 B3 : 6ns@CL2.5
B4 : 5ns@CL2.5 C4 : 5ns@CL3
C5 : 3.75ns@CL3
CC : 5ns@CL3, TRCD3, TRP3 CD : 4ns@CL3
CF : 3.75ns@CL3 (1.9V)

17~18. Customer (Special Handling)

"Customer List Reference"